# REALTEK

**RTL8201F-VB**
**RTL8201FL-VB**
**RTL8201FN-VB**
**RTL8201FR-VB**

# SINGLE-CHIP/PORT 10/100M ETHERNET PHYCEIVER WITH AUTO MDIX

# WAKE-ON-LAN (WOL) APPLICATION NOTE
### (CONFIDENTIAL: Development Partners Only)

**Rev. 1.3**
**24 July 2012**
**Track ID: JATR-3375-16**

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## USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## REVISION HISTORY

| Revision | Release Date | Summary |
|---|---|---|
| 1.0 | 2011/06/23 | First release. |
| 1.1 | 2011/07/27 | Corrected minor typing errors. |
| 1.2 | 2012/06/13 | Corrected Table 22 Page 17, Reg19, Bit [2:0] (PMEB Pulse Width & Active Low/Pulse Low Settings), page 33. |
| 1.3 | 2012/07/24 | Revised section 6.2 Set Wake-Up Frame CRC, page 20. |

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# 1. Introduction

The RTL8201F/FL/FN/FR-VB can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs.

The PME pin needs to be connected with a 4.7k ohm resistor and pulled up to 3.3V or 5V. When the Wake-Up Frame or Magic Packet is sent to the PHY, the PME pin will be set low to notify the system to Wake-Up. The PME pin can accept two waveform formats:

- Active Low Wake-Up (details in section 8.2, page 27)

- Pulse Low Wake-Up (details in section 8.3, page 33)


A Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8201F/FL/FN/FR-VB, e.g., a broadcast, multicast, or unicast packet addressed to the RTL8201F/FL/FN/FR-VB.

- The received Magic Packet does not contain a CRC error.

- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.


A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8201F/FL/FN/FR-VB, e.g., a broadcast, multicast, or unicast address to the current RTL8201F/FL/FN/FR-VB.

- The received Wake-Up Frame does not contain a CRC error.

- The 16-bit CRC of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8201F/FL/FN/FR-VB is configured to allow direct packet wake-up, e.g., a broadcast, multicast, or unicast network packet.

*Note 1: 16-bit CRC: The RTL8201F/FL/FN/FR-VB supports eight long wake-up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^5+1$.*

*Note 2: The RTL8201F/FL/FN/FR-VB provides a 296-bit eFUSE space for MAC programming.*

# 2. Pin Assignments

## 2.1. RTL8201F (32-Pin)
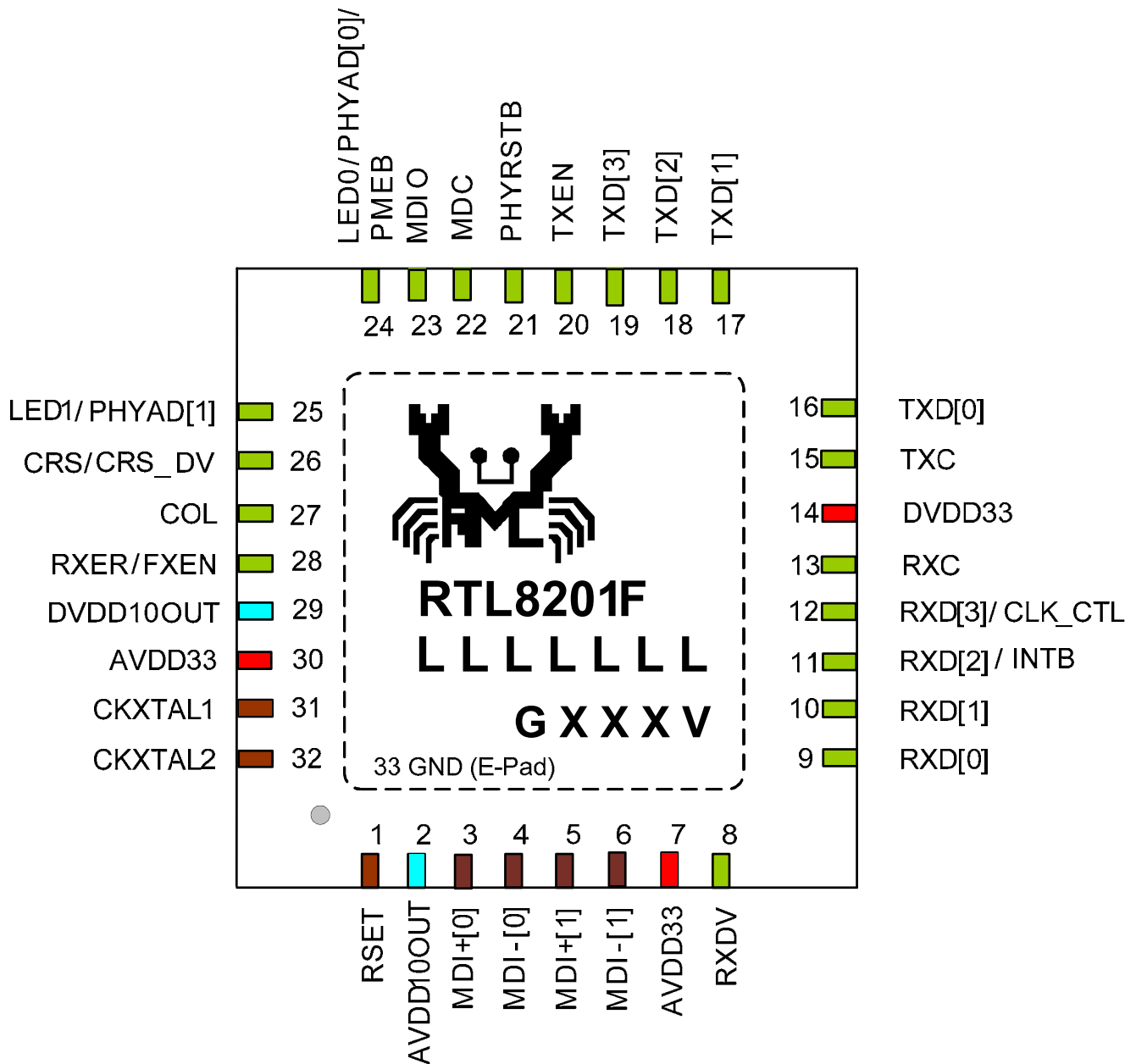


**Figure 1.    RTL8201F QFN-32 Pin Assignments**

## 2.2. RTL8201FL (48-Pin)
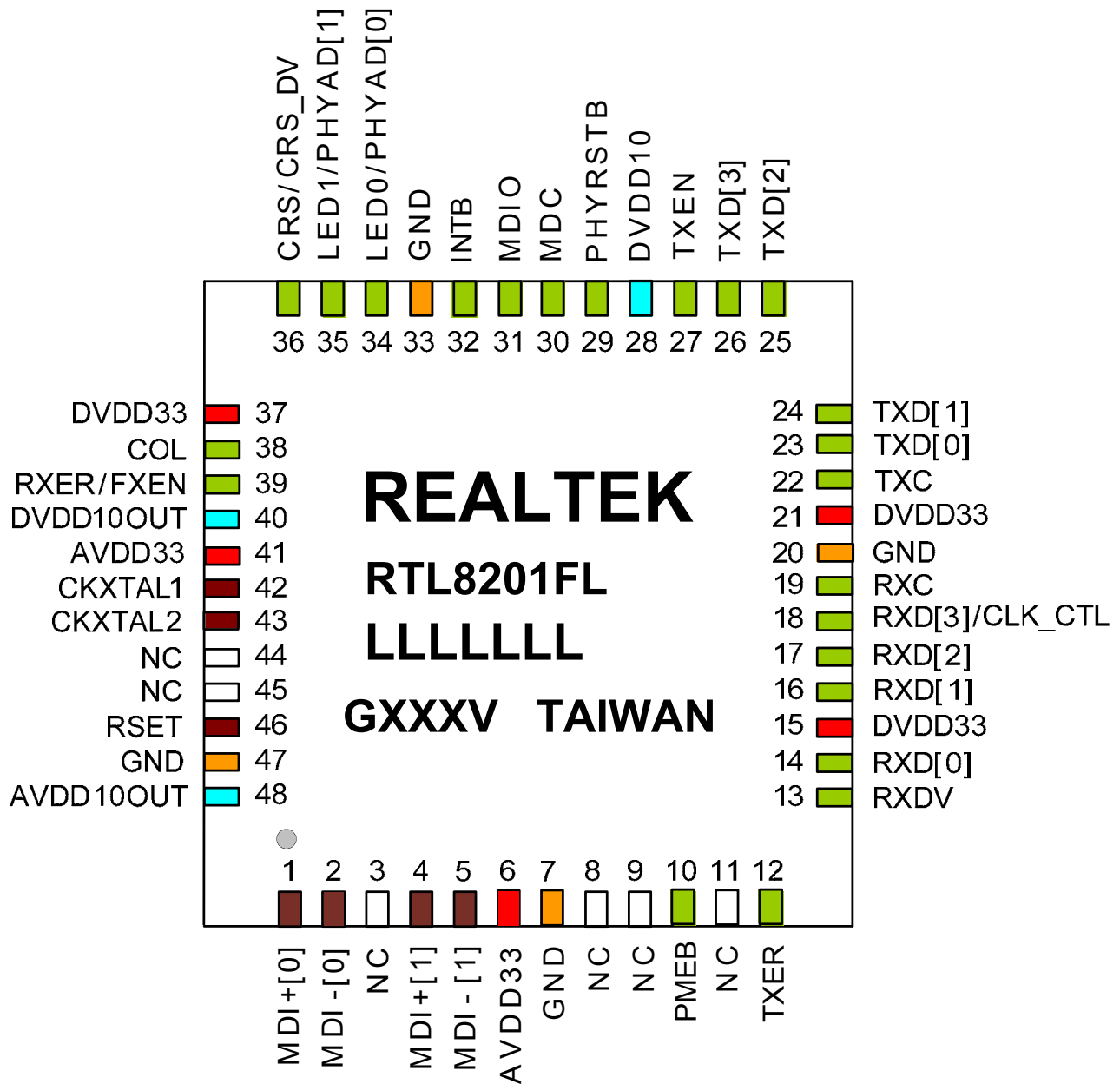


**Figure 2.  RTL8201FL LQFP-48 Pin Assignments**

## 2.3. RTL8201FN (48-Pin)
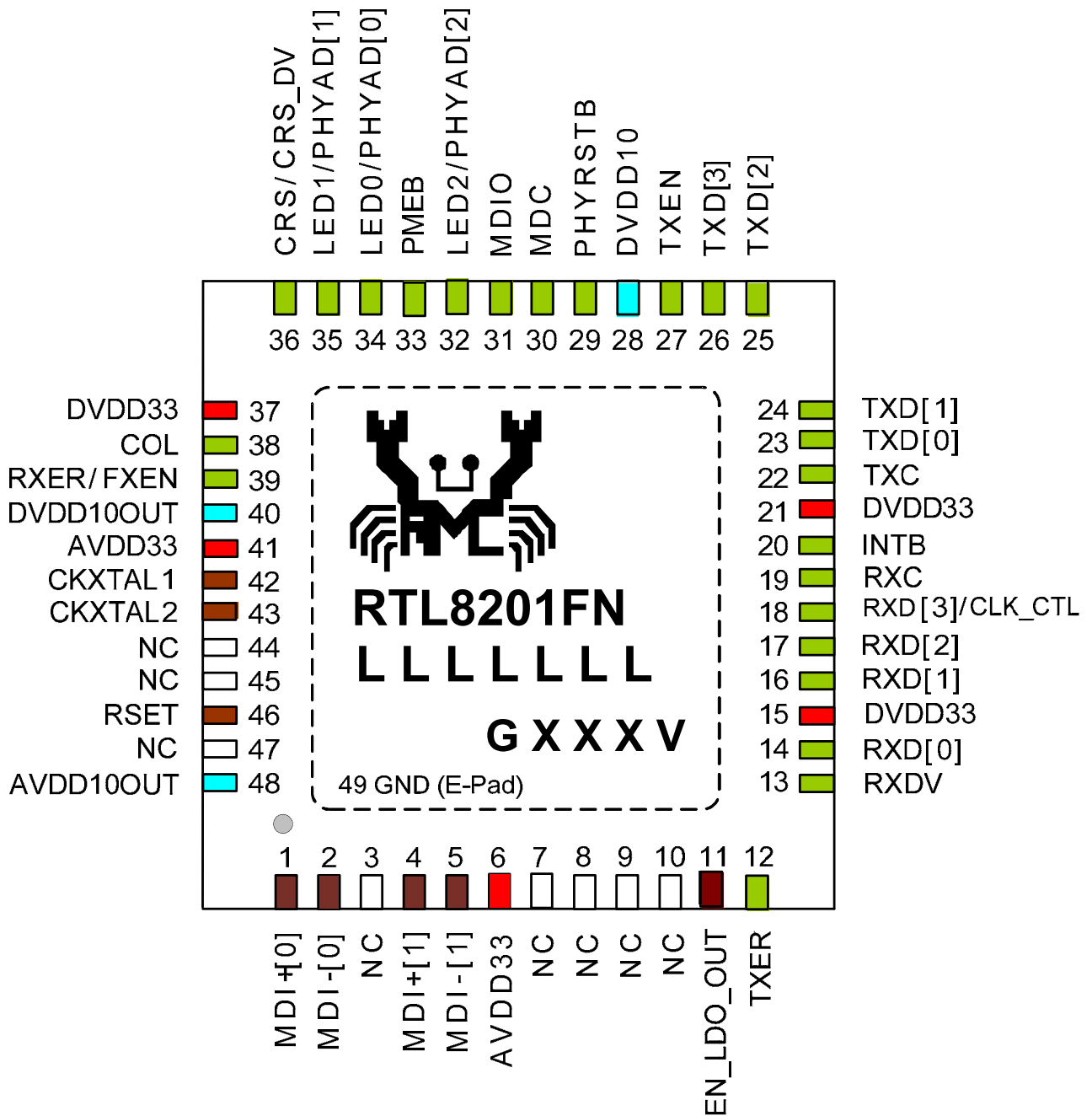


**Figure 3.    RTL8201FN QFN-48 Pin Assignments**

## 2.4. *RTL8201FR (24-Pin)*
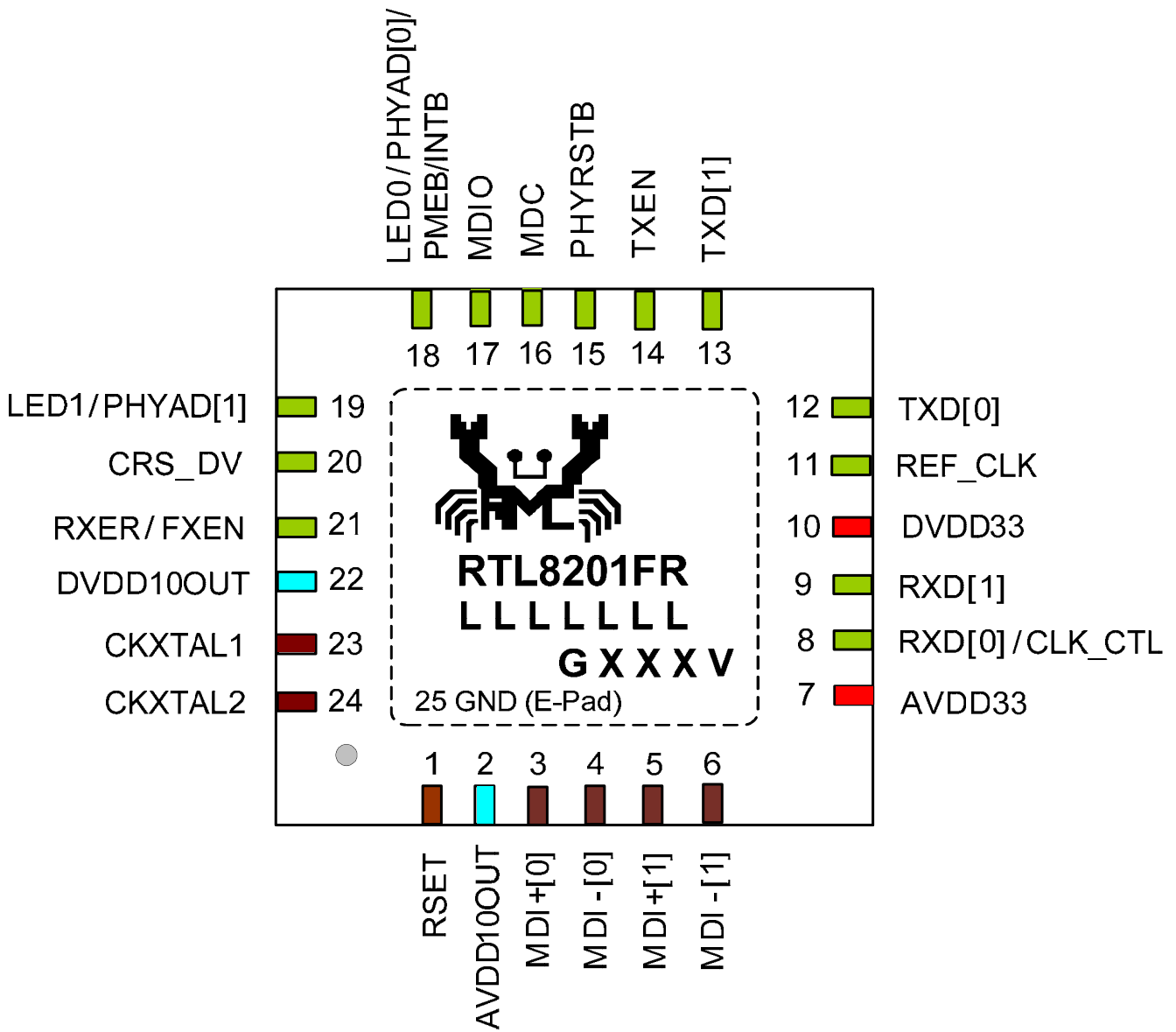


**Figure 4.    RTL8201FR QFN-24 Pin Assignments**

# 3. Wake-On-LAN (WOL) Flow Chart



**Initial Setting**

1. Set MAC Address // Page 18 Reg16~Reg18
2. Set Max packet length//Page 17 Reg17 = 0x1FFF

**Enter WOL**

1. WOL event select and enable
   Page 17 Reg16 bit[15:0]=3FFF //Enable all WOL events
2. Wake up frame select and enable
   Page 8~15 Reg16~Reg23 // Mask of wake-up frame #1~#8
   Page 16 Reg16~Reg23 // 16 bits CRC of wake- up frame #1~#8
3. Speed selection (Suggest change to link at 10M)
4. MII/RMII TX Isolate (Page 7 Reg20 Bit15 for TX Isolate Enable)
5. MII/RMII RX Isolate (Page 17 Reg19 Bit15 for RX Isolate Enable)

**Wait for WOL**

Link change/Magic packet
Wake-up frame/Unicast/Multicast

**PMEB Pin**

No (High)

Yes (Low)

**Exit WOL**

1. Restore to the original link speed
2. MII/RMII TX and RX isolate disable
   (TX isolate disable: Page7 Reg20 bit[15] =0)
   (RX isolate disable: Page17 Reg19 bit[15] =0)
3. Disable all WOL events
   Page 17 Reg16 bit[15:0]=0 //Disable WOL
4. WOL reset
   Page 17 Reg17 bit[15]=1 //Reset WOL

**Finish**

**Figure 5.    Wake-On-LAN (WOL) Flow Chart**

# 4. Wake-On-LAN (WOL) Register Settings (Page 17)

**Enable WOL Link Change Event**

Write Register31, Data=0x0011 //Select page 17

Write Register16, Data=0x2000 //Enable Link Change Event

**Enable WOL Magic Packet Event (Default)**

Write Register31, Data=0x0011 //Select page 17

Write Register16, Data=0x1000 //Enable Magic Packet Event

**Enable WOL Unicast Event**

Write Register31, Data=0x0011 //Select page 17

Write Register16, Data=0x0400 //Enable Unicast Event

**Enable WOL Multicast Event**

Write Register31, Data=0x0011 //Select page 17

Write Register16, Data=0x0200 //Enable Multicast Event

**Enable WOL Broadcast Event**

Write Register31, Data=0x0011 //Select page 17

Write Register16, Data=0x0100 //Enable Broadcast

**Enable WOL Wake-Up Frame Event**

Write Register31, Data=0x0011 //Select page 17

Write Register16, Data=0x0001 //Enable Wake-Up Frame 0 Event

Write Register16, Data=0x0002 //Enable Wake-Up Frame 1 Event

Write Register16, Data=0x0004 //Enable Wake-Up Frame 2 Event

Write Register16, Data=0x0008 //Enable Wake-Up Frame 3 Event

Write Register16, Data=0x0010 //Enable Wake-Up Frame 4 Event

Write Register16, Data=0x0020 //Enable Wake-Up Frame 5 Event

Write Register16, Data=0x0040 //Enable Wake-Up Frame 6 Event

Write Register16, Data=0x0080 //Enable Wake-Up Frame 7 Event

**Enable All WOL Events**

Write Register31, Data=0x0011 //Select page 17

Write Register16, Data=0xffff //Enable all Wake-On-LAN Events

**Return to Page 0**

Write Register31, Data=0x0000 //Return to page 0

**Table 1.    Page 17, Register 16**

| Bit | Name | Type | Description | Default Value |
|-----|------|------|-------------|---------------|
| 15:14 | - | RW | Reserved | 0 |
| 13 | linkchg_wol_en | RW | PMEB Asserted due to Detection of a Change in the Network Link State | 0 |
| 12 | magic_en | RW | PMEB Asserted due to Receipt of a Magic Packet | 1 |
| 11 | awf_en | RW | PMEB Asserted due to Receipt of a Network Packet | 0 |
| 10 | uwf_en | RW | PMEB Asserted due to Receipt of a Network Unicast Packet that was Sent to a Local Device | 0 |
| 9 | mwf_en | RW | PMEB Asserted due to Receipt of a Network Multicast Packet that was Sent to a Local Device | 0 |
| 8 | bwf_en | RW | PMEB Asserted due to Receipt of a Network Broadcast Packet | 0 |
| 7 | enwakeup7 | RW | PMEB Asserted due to Receipt of Network Wake-Up Frame #7 | 0 |
| 6 | enwakeup6 | RW | PMEB Asserted due to Receipt of Network Wake-Up Frame #6 | 0 |
| 5 | enwakeup5 | RW | PMEB Asserted due to Receipt of Network Wake-Up Frame #5 | 0 |
| 4 | enwakeup4 | RW | PMEB Asserted due to Receipt of Network Wake-Up Frame #4 | 0 |
| 3 | enwakeup3 | RW | PMEB Asserted due to Receipt of Network Wake-Up Frame #3 | 0 |
| 2 | enwakeup2 | RW | PMEB Asserted due to Receipt of Network Wake-Up Frame #2 | 0 |
| 1 | enwakeup1 | RW | PMEB Asserted due to Receipt of Network Wake-Up Frame #1 | 0 |
| 0 | enwakeup0 | RW | PMEB asserted due to Receipt of Network Wake-Up Frame #0 | 0 |

**Reset and Maximum Packet Bytes Register**

Write Page17 Register17, Data=0x9fff //reset Wake-On-LAN Event (The PMEB pin goes low when a WOL event occurs; write Page17 Register17, Data=0x9fff to reset the PMEB pin back to default status).

*Note: The registers remain constant when a WOL reset is enabled. A power on reset or hardware reset can reset all registers back to original values.*

**Table 2.    Page 17, Register 17**

| Bit | Name | Type | Description | Default Value |
|-----|------|------|-------------|---------------|
| 15 | rg_rst | W | Reset Wake-On-LAN via Register | 0 |
| 14:0 | Rmsq | RW | Defines the Maximum Received Packet Bytes | 0 |

# 5. Unique Physical Address & Multicast Register (Registers 16~22)

The RTL8201FN/FL/F/FR-VB supports unicast and multicast events. For unicast application it needs to write the MAC address to PHY register 16~18 (page 18).

Refer to Figure 7, page 11 and Table 3, page 12 for multicast application.

**//Unicast Example: Set MAC address=00:12:34:56:78:9A**

Write Register31, Data=0x0012 //Select page 18

Write Register16, Data=0x1200 (bit [15:8]: MAC address byte2; bit [7:0]: MAC address byte1)

Write Register17, Data=0x5634 (bit [15:8]: MAC address byte4; bit [7:0]: MAC address byte3)

Write Register18, Data=0x9a78 (bit [15:8]: MAC address byte6; bit [7:0]: MAC address byte5)
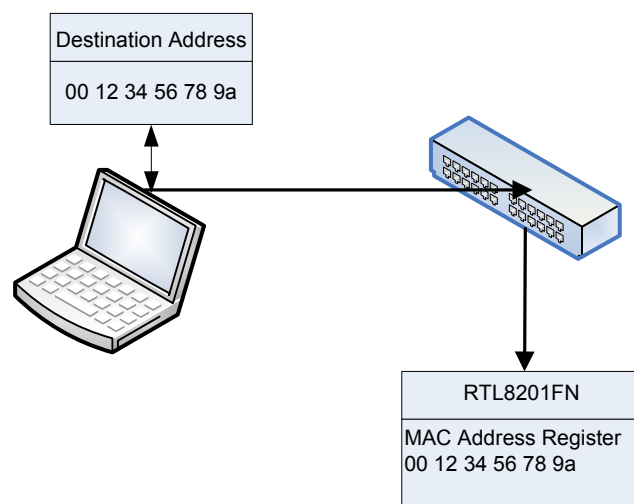


**Figure 6.     Unicast Application**

**//Multicast Example: Set Multicast register=01:00:00:00:00:00:00:00**

(Destination address is 01, 02, 3C, 00, 00, 00)

Write Register31, Data=0x0012 //Select page 18

Write Register19, Data=0x0000

Write Register20, Data=0x0000

Write Register21, Data=0x0000

Write Register22, Data=0x0100
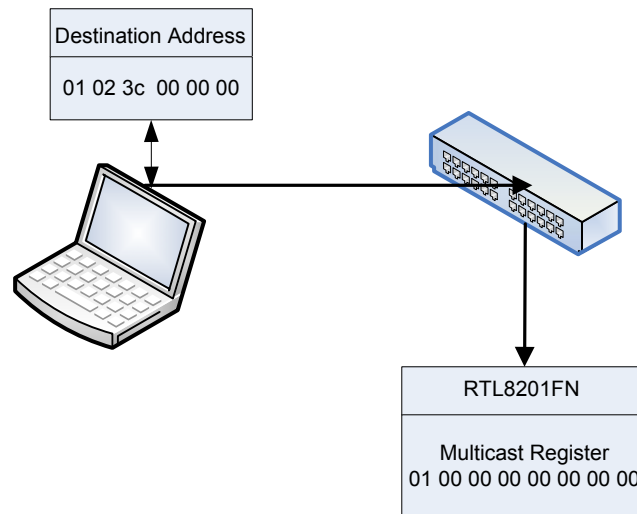


**Figure 7.    Multicast Application**

**Table 3.    Multicast Pattern and Register**

| No. | Multicast Pattern | Multicast Register |
|---|---|---|
| 0 | 01, 02, 3C, 00, 00, 00 | 01, 00, 00, 00, 00, 00, 00, 00 |
| 1 | 01, 02, 07, 00, 00, 00 | 02, 00, 00, 00, 00, 00, 00, 00 |
| 2 | 01, 02, 1F, 00, 00, 00 | 04, 00, 00, 00, 00, 00, 00, 00 |
| 3 | 01, 02, 24, 00, 00, 00 | 08, 00, 00, 00, 00, 00, 00, 00 |
| 4 | 01, 02, 28, 00, 00, 00 | 10, 00, 00, 00, 00, 00, 00, 00 |
| 5 | 01, 02, 13, 00, 00, 00 | 20, 00, 00, 00, 00, 00, 00, 00 |
| 6 | 01, 02, 0B, 00, 00, 00 | 40, 00, 00, 00, 00, 00, 00, 00 |
| 7 | 01, 02, 30, 00, 00, 00 | 80, 00, 00, 00, 00, 00, 00, 00 |
| 8 | 01, 02, 0D, 00, 00, 00 | 00, 01, 00, 00, 00, 00, 00, 00 |
| 9 | 01, 02, 36, 00, 00, 00 | 00, 02, 00, 00, 00, 00, 00, 00 |
| 10 | 01, 02, 2E, 00, 00, 00 | 00, 04, 00, 00, 00, 00, 00, 00 |
| 11 | 01, 02, 15, 00, 00, 00 | 00, 08, 00, 00, 00, 00, 00, 00 |
| 12 | 01, 02, 19, 00, 00, 00 | 00, 10, 00, 00, 00, 00, 00, 00 |
| 13 | 01, 02, 22, 00, 00, 00 | 00, 20, 00, 00, 00, 00, 00, 00 |
| 14 | 01, 02, 3A, 00, 00, 00 | 00, 40, 00, 00, 00, 00, 00, 00 |
| 15 | 01, 02, 01, 00, 00, 00 | 00, 80, 00, 00, 00, 00, 00, 00 |
| 16 | 01, 02, 21, 00, 00, 00 | 00, 00, 01, 00, 00, 00, 00, 00 |
| 17 | 01, 02, 1A, 00, 00, 00 | 00, 00, 02, 00, 00, 00, 00, 00 |
| 18 | 01, 02, 02, 00, 00, 00 | 00, 00, 04, 00, 00, 00, 00, 00 |
| 19 | 01, 02, 39, 00, 00, 00 | 00, 00, 08, 00, 00, 00, 00, 00 |
| 20 | 01, 02, 35, 00, 00, 00 | 00, 00, 10, 00, 00, 00, 00, 00 |
| 21 | 01, 02, 0E, 00, 00, 00 | 00, 00, 20, 00, 00, 00, 00, 00 |
| 22 | 01, 02, 16, 00, 00, 00 | 00, 00, 40, 00, 00, 00, 00, 00 |
| 23 | 01, 02, 2D, 00, 00, 00 | 00, 00, 80, 00, 00, 00, 00, 00 |
| 24 | 01, 02, 10, 00, 00, 00 | 00, 00, 00, 01, 00, 00, 00, 00 |
| 25 | 01, 02, 2B, 00, 00, 00 | 00, 00, 00, 02, 00, 00, 00, 00 |
| 26 | 01, 02, 33, 00, 00, 00 | 00, 00, 00, 04, 00, 00, 00, 00 |
| 27 | 01, 02, 08, 00, 00, 00 | 00, 00, 00, 08, 00, 00, 00, 00 |

| No. | Multicast Pattern | Multicast Register |
|:---:|:---:|:---:|
| 28 | 01, 02, 04, 00, 00, 00 | 00, 00, 00, 10, 00, 00, 00, 00 |
| 29 | 01, 02, 3F, 00, 00, 00 | 00, 00, 00, 20, 00, 00, 00, 00 |
| 30 | 01, 02, 27, 00, 00, 00 | 00, 00, 00, 40, 00, 00, 00, 00 |
| 31 | 01, 02, 1C, 00, 00, 00 | 00, 00, 00, 80, 00, 00, 00, 00 |
| 32 | 01, 02, 37, 00, 00, 00 | 00, 00, 00, 00, 01, 00, 00, 00 |
| 33 | 01, 02, 0C, 00, 00, 00 | 00, 00, 00, 00, 02, 00, 00, 00 |
| 34 | 01, 02, 14, 00, 00, 00 | 00, 00, 00, 00, 04, 00, 00, 00 |
| 35 | 01, 02, 2F, 00, 00, 00 | 00, 00, 00, 00, 08, 00, 00, 00 |
| 36 | 01, 02, 23, 00, 00, 00 | 00, 00, 00, 00, 10, 00, 00, 00 |
| 37 | 01, 02, 18, 00, 00, 00 | 00, 00, 00, 00, 20, 00, 00, 00 |
| 38 | 01, 02, 00, 00, 00, 00 | 00, 00, 00, 00, 40, 00, 00, 00 |
| 39 | 01, 02, 3B, 00, 00, 00 | 00, 00, 00, 00, 80, 00, 00, 00 |
| 40 | 01, 02, 06, 00, 00, 00 | 00, 00, 00, 00, 00, 01, 00, 00 |
| 41 | 01, 02, 3D, 00, 00, 00 | 00, 00, 00, 00, 00, 02, 00, 00 |
| 42 | 01, 02, 25, 00, 00, 00 | 00, 00, 00, 00, 00, 04, 00, 00 |
| 43 | 01, 02, 1E, 00, 00, 00 | 00, 00, 00, 00, 00, 08, 00, 00 |
| 44 | 01, 02, 12, 00, 00, 00 | 00, 00, 00, 00, 00, 10, 00, 00 |
| 45 | 01, 02, 29, 00, 00, 00 | 00, 00, 00, 00, 00, 20, 00, 00 |
| 46 | 01, 02, 31, 00, 00, 00 | 00, 00, 00, 00, 00, 40, 00, 00 |
| 47 | 01, 02, 0A, 00, 00, 00 | 00, 00, 00, 00, 00, 80, 00, 00 |
| 48 | 01, 02, 2A, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 01, 00 |
| 49 | 01, 02, 11, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 02, 00 |
| 50 | 01, 02, 09, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 04, 00 |
| 51 | 01, 02, 32, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 08, 00 |
| 52 | 01, 02, 3E, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 10, 00 |
| 53 | 01, 02, 05, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 20, 00 |
| 54 | 01, 02, 1D, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 40, 00 |
| 55 | 01, 02, 26, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 80, 00 |
| 56 | 01, 02, 1B, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 01 |

| No. | Multicast Pattern | Multicast Register |
|---|---|---|
| 57 | 01, 02, 20, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 02 |
| 58 | 01, 02, 38, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 04 |
| 59 | 01, 02, 03, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 08 |
| 60 | 01, 02, 0F, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 10 |
| 61 | 01, 02, 34, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 20 |
| 62 | 01, 02, 2C, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 40 |
| 63 | 01, 02, 17, 00, 00, 00 | 00, 00, 00, 00, 00, 00, 00, 80 |

**Table 4.    Page 18**

| Reg | Bit | Name | Type | Description | Default Value |
|---|---|---|---|---|---|
| 16 | 15:0 | uni_phy_addr[15:0] | RW/EFUS | Unique Physical Address (MAC Address) | 0 |
| 17 | 15:0 | uni_phy_addr[31:16] | RW/EFUS | Unique Physical Address (MAC Address) | 0 |
| 18 | 15:0 | uni_phy_addr[47:32] | RW/EFUS | Unique Physical Address (MAC Address) | 0 |
| 19 | 15:0 | multicast_register[15:0] | RW | Multicast Register | 0 |
| 20 | 15:0 | multicast_register[31:16] | RW | Multicast Register | 0 |
| 21 | 15:0 | multicast_register[47:32] | RW | Multicast Register | 0 |
| 22 | 15:0 | multicast_register[63:48] | RW | Multicast Register | 0 |

# 6. Wake-Up Frame Mask & CRC Setting (Page 8~16, Register 16~23)

Pages 8 to 15 are Wake-Up Frame mask registers that support Wake-Up Frame 0 to 7.

Page 16 is the Wake-Up Frame CRC register.

## 6.1. Set Wake-Up Frame Mask

Example: Set Wake-Up Frame Mask=0x00 03 C0 00 20 30 00

Packet data: (Red color is the MASK)

```
           LSB       MSB
          0 1 2 3   0 1 2 3
```

|  |  |  |  |
|---|---|---|---|
| 0 | 0 | 0 | 3(1100) |
| 00 1d 72 1c | b6 c6 c8 0a | a9 65 8c d5 | 08 00 45 00 |
| 0 | 2(0100) | 0 | 0 |
| 00 3c 77 d9 | 00 02 80 01 | 3f 8a c0 a8 | 01 0b c0 a8 |
| 0 | C(0011) | 3(1100) | 0 |
| 01 02 08 00 | 4d 5a 22 01 | 3f a1 61 62 | 63 64 65 66 |

```
67 68 69 6a      6b 6c 6d 6e      6f 70 71 72      73 74 75 76

77 61 62 63      64 65 66 67      68 69
```
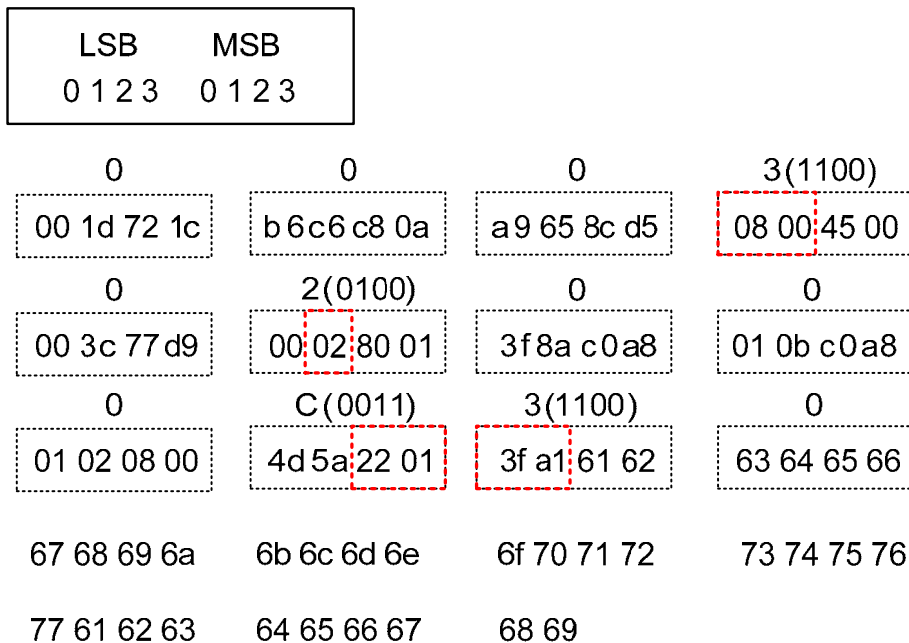
**Figure 8.    Set Wake-Up Frame Mask**

**Wake On LAN (WOL)**
**Application Note**

Masked Bytes are used to calculate the CRC: 0x08, 0x00, 0x02, 0x22, 0x01, 0x3f, 0xa1

//Example: Write page8 for Wake-Up Frame 0 mask:

Write Register31, Data=0x0008 //Select page 8 (Wake-Up Frame 0)

Write Register16, Data=0x3000

Write Register17, Data=0x0020

Write Register18, Data=0x03c0

Write Register19, Data=0x0000

Write Register20, Data=0x0000

Write Register21, Data=0x0000

Write Register22, Data=0x0000

Write Register23, Data=0x0000

**Table 5.    Page 8 (Wake-Up Frame 0)**

| Reg | Bit | Name | Type | Description | Default Value |
|---|---|---|---|---|---|
| 16 | 15:0 | byte_msk_wf0[15:0] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf0[31:16] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf0[47:32] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf0[63:48] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |
| 20 | 15:0 | byte_msk_wf0[79:64] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf0[95:80] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf0[111:96] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf0[127:112] | RW | Byte Masks of Wake-Up Frame #0 for Power Management | 0 |

**Table 6.     Page 9 (Wake-Up Frame 1)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 16 | 15:0 | byte_msk_wf1[15:0] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf1[31:16] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf1[47:32] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf1[63:48] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |
| 20 | 15:0 | byte_msk_wf1[79:64] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf1[95:80] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf1[111:96] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf1[127:112] | RW | Byte Masks of Wake-Up Frame #1 for Power Management | 0 |

**Table 7.     Page 10 (Wake-Up Frame 2)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 16 | 15:0 | byte_msk_wf2[15:0] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf2[31:16] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf2[47:32] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf2[63:48] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |
| 20 | 15:0 | byte_msk_wf2[79:64] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf2[95:80] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf2[111:96] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf2[127:112] | RW | Byte Masks of Wake-Up Frame #2 for Power Management | 0 |

**Table 8.     Page 11 (Wake-Up Frame 3)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 16 | 15:0 | byte_msk_wf3[15:0] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf3[31:16] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf3[47:32] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf3[63:48] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 20 | 15:0 | byte_msk_wf3[79:64] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf3[95:80] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf3[111:96] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf3[127:112] | RW | Byte Masks of Wake-Up Frame #3 for Power Management | 0 |

**Table 9.     Page 12 (Wake-Up Frame 4)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 16 | 15:0 | byte_msk_wf4[15:0] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf4[31:16] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf4[47:32] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf4[63:48] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |
| 20 | 15:0 | byte_msk_wf4[79:64] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf4[95:80] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf4[111:96] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf4[127:112] | RW | Byte Masks of Wake-Up Frame #4 for Power Management | 0 |

**Table 10.    Page 13 (Wake-Up Frame 5)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 16 | 15:0 | byte_msk_wf5[15:0] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf5[31:16] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf5[47:32] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf5[63:48] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |
| 20 | 15:0 | byte_msk_wf5[79:64] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf5[95:80] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf5[111:96] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf5[127:112] | RW | Byte Masks of Wake-Up Frame #5 for Power Management | 0 |

**Table 11.   Page 14 (Wake-Up Frame 6)**

| Reg | Bit | Name | Type | Description | Default Value |
|---|---|---|---|---|---|
| 16 | 15:0 | byte_msk_wf6[15:0] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf6[31:16] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf6[47:32] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf6[63:48] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |
| 20 | 15:0 | byte_msk_wf6[79:64] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf6[95:80] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf6[111:96] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf6[127:112] | RW | Byte Masks of Wake-Up Frame #6 for Power Management | 0 |

**Table 12.   Page 15 (Wake-Up Frame 7)**

| Reg | Bit | Name | Type | Description | Default Value |
|---|---|---|---|---|---|
| 16 | 15:0 | byte_msk_wf7[15:0] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |
| 17 | 15:0 | byte_msk_wf7[31:16] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |
| 18 | 15:0 | byte_msk_wf7[47:32] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |
| 19 | 15:0 | byte_msk_wf7[63:48] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |
| 20 | 15:0 | byte_msk_wf7[79:64] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |
| 21 | 15:0 | byte_msk_wf7[95:80] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |
| 22 | 15:0 | byte_msk_wf7[111:96] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |
| 23 | 15:0 | byte_msk_wf7[127:112] | RW | Byte Masks of Wake-Up Frame #7 for Power Management | 0 |

## 6.2. Set Wake-Up Frame CRC

//Example: Set Wake-Up Frame CRC=0xdf6b

Write Register31, Data=0x0010 //Select page 16

Write Register16, Data=0xdf6b //Set Wake-Up Frame #0 CRC=0xdf6b

**Table 13.    Page 16 (WOL_Wake_CRC)**

| Reg | Bit | Name | Type | Description | Default Value |
|---|---|---|---|---|---|
| 16 | 15:0 | wfcrc0 | RW | 16-Bit CRC of Wake-Up Frame #0 | 0 |
| 17 | 15:0 | wfcrc1 | RW | 16-Bit CRC of Wake-Up Frame #1 | 0 |
| 18 | 15:0 | wfcrc2 | RW | 16-Bit CRC of Wake-Up Frame #2 | 0 |
| 19 | 15:0 | wfcrc3 | RW | 16-Bit CRC of Wake-Up Frame #3 | 0 |
| 20 | 15:0 | wfcrc4 | RW | 16-Bit CRC of Wake-Up Frame #4 | 0 |
| 21 | 15:0 | wfcrc5 | RW | 16-Bit CRC of Wake-Up Frame #5 | 0 |
| 22 | 15:0 | wfcrc6 | RW | 16-Bit CRC of Wake-Up Frame #6 | 0 |
| 23 | 15:0 | wfcrc7 | RW | 16-Bit CRC of Wake-Up Frame #7 | 0 |

**Set Wake-Up Frame for WOL example as follows:**

1. Set maximum packet and WOL event

Write Register31, Data = 0x0011 //Select Page 17

Write Register17, Data=0x9FFF //Maximum packet length

Write Register16, Data =0x0001 //Enable WOL Wake-Up Frame 0 event

2. Set MAC address = 00:12:34:56:78:9A

Write Register31, Data =0x0012 //Select page 18

Write Register16, Data =0x1200

Write Register17, Data =0x5634

Write Register18, Data =0x9a78

3. Set Wake-Up Frame mask; Wake-Up Frame mask = 0x0000_03C0_0020_3000

Write Register31, Data=0x0008 //Select page 8

Write Register16, Data =0x3000

Write Register17, Data =0x0020

Write Register18, Data =0x03C0

Write Register19, Data =0x0000

Write Register20, Data =0x0000

Write Register21, Data =0x0000

Write Register22, Data =0x0000

Write Register23, Data =0x0000


4. Set Wake-Up Frame CRC

Write Register31, Data =0x0010 //Select page 16

Write Register16, Data =0xdf6b //Set Wake-Up Frame #0 CRC = 0xdf6b


5. Enable MII/RMII TX isolation for power saving

Write Register31, Data =0x0007 //Select page 7

Write Register20, Data =0x90d3 //Enable TX isolation


6. Enable MII/RMII RX isolation for power saving

Write Register31, Data =0x0011 //Select page 17

Write Register19, Data =0x8002 //Enable RX isolation

# 7. Wake-On-LAN (WOL) Pin Types

The signal type codes below are used in the following tables:

I:   Input

O:   Output

IO:   Bi-Directional Input and Output

PU:   Internal Pull Up during Power On Reset

LI:   Latched Input during Power Up or Reset

L:   Low

PD:   Internal Pull Down during Power On Reset

## 7.1.   MII Interface

**Table 14.   MII Interface**

| Name | Type | Normal | | | WOL Enable |
|------|------|--------|------|------|------------|
| | | **100M** | **10M** | **Idle** | |
| TXC | O/PD | 25M CLK Output | 2.5M CLK Output | 2.5M CLK Output | O (2.5M/25M)/L/PD (Note 1) |
| TXEN | I/PD | I | I | I | I/PD |
| TXD[0:3] | I/PD | I | I | I | I/PD |
| RXC | O/PD | 25M CLK Output | 2.5M CLK Output | 2.5M CLK Output | O (2.5M/25M)/L (Note 2) |
| COL | LI/O/PD | O | O | O | O or L (Note 2) |
| CRS | O/PD | O | O | O | O or L (Note 2) |
| RXDV | LI/O/PD | O | O | O | O or L (Note 2) |
| RXD[0:3] | O/PD | O | O | O | O or L (Note 2) |
| RXER | LI/O/PD | O | O | O | O or L (Note 2) |
| MDC | I/PU | I | I | I | I/PU |
| MDIO | IO/PU | IO | IO | IO | IO/PU |

*Note 1: If TX Isolate=1, then TXC is halted and the TXC pin type is 'L'.*

   *To set the TXC pin type to 'PD', set page0, register0, bit10=0.*

*Note 2: If RX Isolate=1, Rx_CLK isolate=1, all MII RX interfaces are stopped and the MII RX pin type is Low.*

   *If RX Isolate=1, Rx_CLK isolate=0, the RXC signal is toggled. The other MII RX interfaces are stopped and the*

   *MII RX pin type is Low.*

   *If RX Isolate=0, Rx_CLK isolate=0, all MII RX signals are toggled.*

## 7.2. RMII Interface

**Table 15.    RMII Interface**

| Name | Type | Normal | | | WOL Enable |
|---|---|---|---|---|---|
| | | **100M** | **10M** | **Idle** | |
| TXC (REF_CLK) (Note 1) | IO/PD | 50M CLK Input/Output | 50M CLK Input/Output | 50M CLK Input/Output | I/O (50M) (Note 2) |
| TXEN | I/PD | I | I | I | I/PD |
| TXD[0:1] | I/PD | I | I | I | I/PD |
| CRS_DV | O/PD | O | O | O | O or L (Note 3) |
| RXD[0:1] | O/PD | O | O | O | O or L (Note 3) |
| RXER | LI/O/PD | O | O | O | O or L (Note 3) |
| MDC | I/PU | I | I | I | I/PU |
| MDIO | IO/PU | IO | IO | IO | IO/PU |

*Note 1: If TXC (REF_CLK) is in input mode (MAC to PHY), the REF_CLK does not stop when WOL is enabled.*

*Note 2: When REF_CLK is in output mode (PHY to MAC), the REF_CLK never stops (always toggling; 50MHz output).*

   *To set the TXC pin type to 'PD', set page0, register0, bit10=1.*

*Note 3: If RX Isolate=1, all RMII RX interfaces are stopped and the RMII RX pin type is Low.*

# 8. Magic Packet/Wake-Up Frame Wakeup

**Magic Packet Format**

6 * FFh + MISC (can be none) + 16 * DID (Destination ID)

**Wake-Up Frame Format**

16-bit CRC of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern by the local machine's OS.

**Other Wake-Up Frame Types are:**

- Broadcast: Wakes on Ethernet Broadcast of FF FF FF FF FF FF

- Unicast: Wakes if the header of the packet includes the Device Under Test (DUT) MAC Address (i.e., 11:82:07:BC:13:70)

- Multicast: Wakes if the header of the packet includes the DUT MAC Address (i.e., 11:82:07:BC:13:70)

# 8.1. *Wake-On-LAN (WOL) Circuit*

The RTL8201F/FL/FN/FR-VB can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The PMEB pin must be connected with a 4.7k-ohm resistor and pulled up to 3.3V.

See the following sections for PMEB pin function selection in the RTL8201F-VB and RTL8201FR-VB. No PMEB pin function selection is required in the RTL8201FL-VB and RTL8201FN-VB models.

## 8.1.1. RTL8201F PMEB Pin Function Selection

Method 1: RXD [1] PIN external weakly pulled high

Method 2: Write page7, register19, bit10=1
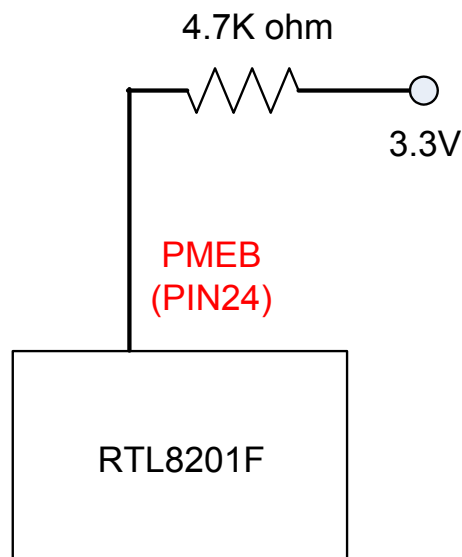


**Figure 9. RTL8201F Wake-On-LAN (WOL) Circuit**

## 8.1.2. RTL8201FR PMEB Pin Function Selection

Method 1: RXD [1] PIN external weakly pulled high

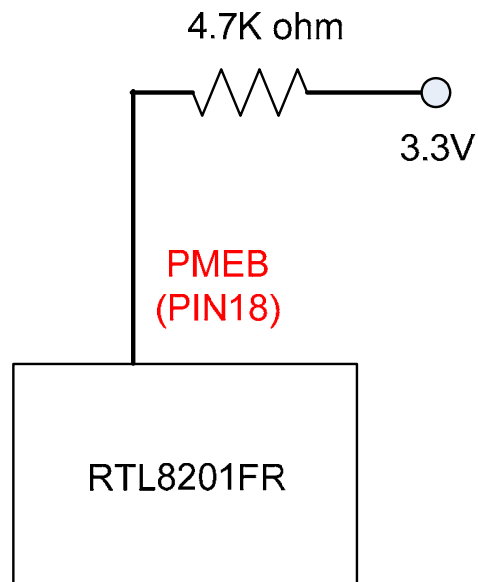Method 2: Write page7, register19, bit10=1



**Figure 10.   RTL8201FR Wake-On-LAN (WOL) Circuit**

# 8.2. Active Low Wakeup

For enhanced PHY power saving, the RTL8201FN/FL/F/FR-VB supports the MII/RMII Interface RX isolation feature for isolation between PHY and MAC in WOL mode. The MII/RMII pins will be output low when RX isolation is enabled (via register; see Table 16).

**Table 16. Page 17, Reg19, Bit15 (RX Isolate Enable) (Active Low)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 19 | 15 | Rg_wol_rx_iso_en | RW | 0: Disable MII/RMII RX Isolate in WOL <br> 1: Enable MII/RMII RX Isolate in WOL | 0 |



T1: MII RX pins disable time (maximum)
T2: MII RX pins enable time (maximum)
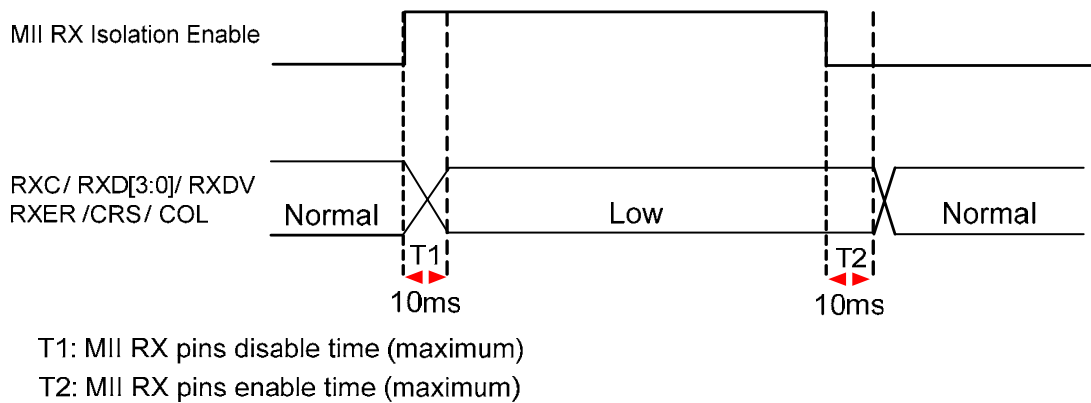
**Figure 11. MII RX Isolation Timing**



T1: RMII RX pins disable time (maximum)
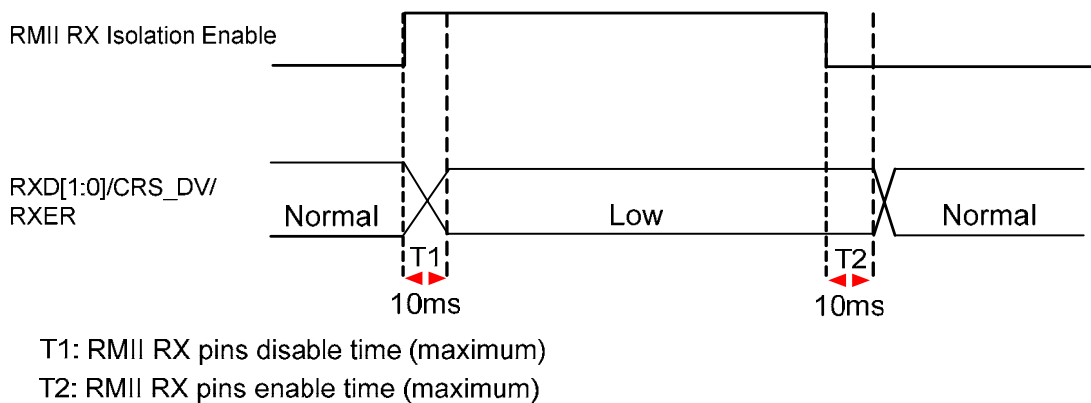T2: RMII RX pins enable time (maximum)

**Figure 12. RMII RX Isolation Timing**

**Table 17.    Page 17, Reg19, Bit14 (RXC Halt/Toggle Selection) (Active Low)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 19 | 14 | Rg_wol_rxc_on | RW | Force MII Mode RXC ON when MII RX Isolate is Enabled<br>1: RXC toggle<br>0: RXC Halt | 0 |

**Table 18.    Page 7, Reg20, Bit15 (TX Isolate Enable) (Active Low)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 20 | 15 | Rg_tx_iso_en | RW | Isolate MII/RMII TX when TX Idle<br>*Note: TX isolate can be used when the TX path is idle (not only for WOL).* | 0 |

# 8.2.1. RX Isolate=1 (TX may or may not be set to isolated)

**MII Mode -- PMEB Active Low After Receiving Magic Packet or Wake-Up Frame**
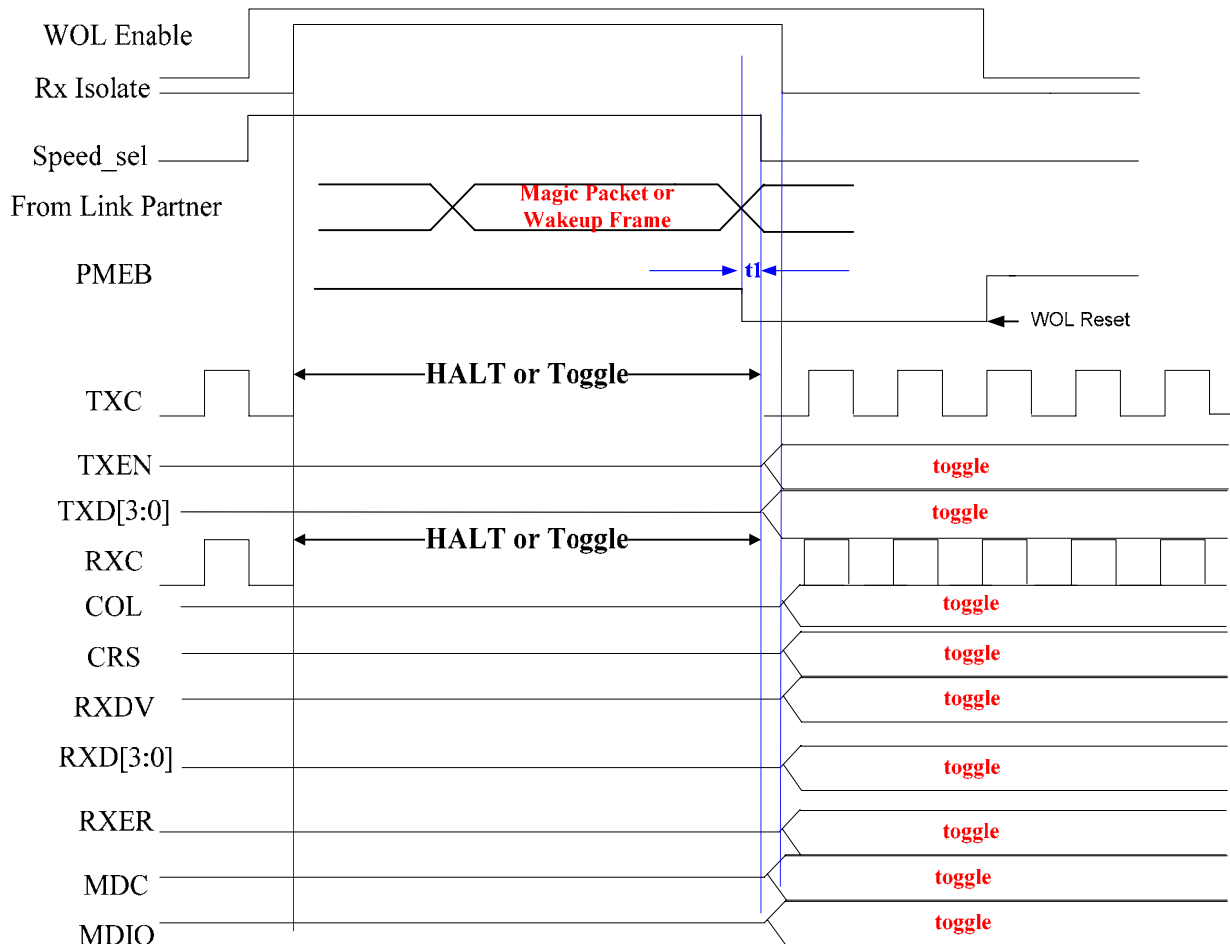
**(Not Available for the RTL8201FR-VB)**



**Figure 13.   WOL Waveform with RX Isolate=1 in MII Mode (Active Low)**

*Note 1: Assumes that MAC TXEN, TXD [3:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: TXC and RXC can be halted or kept toggling in MII mode via register settings.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

*Note 5: PMEB Pin should be reset at WOL disable.*
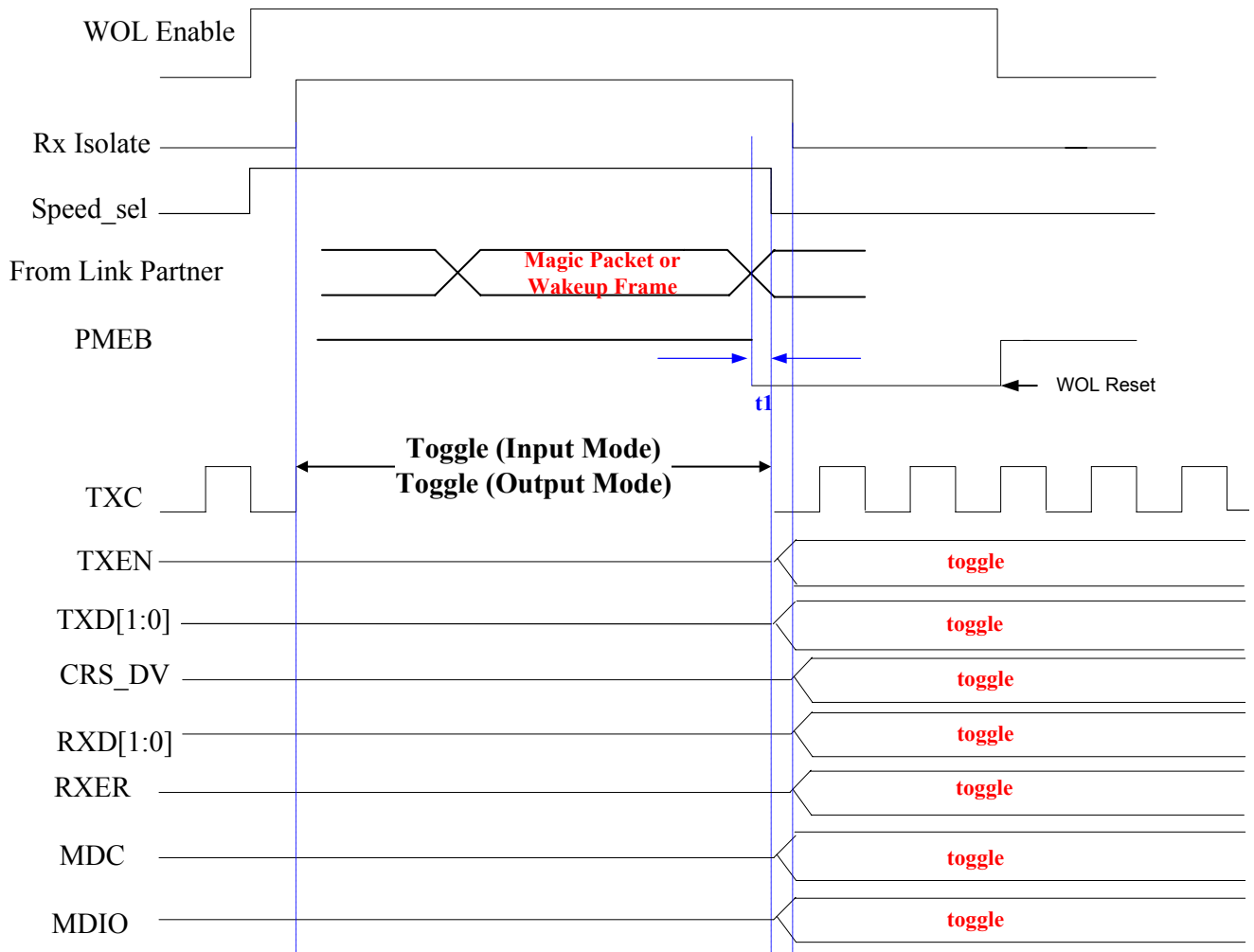
*Note 6: PHYRSTB will be pulled high during WOL operation.*

**RMII Mode -- PMEB Active Low After Receiving Magic Packet or Wake-Up Frame**



**Figure 14.   WOL Waveform with RX Isolate=1 in RMII Mode (Active Low)**

*Note 1: Assumes that MAC TXEN, TXD [1:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: TXC cannot be halted in TXC input mode. TXC can be halted or kept toggling when TXC is in output mode.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

*Note 5: PMEB Pin should be reset at WOL disable.*

*Note 6: PHYRSTB will be pulled high during WOL operation.*

## 8.2.2.    RX Isolate=0 (TX Isolate=0)

**MII Mode -- PMEB Active Low After Receiving Magic Packet or Wake-Up Frame**

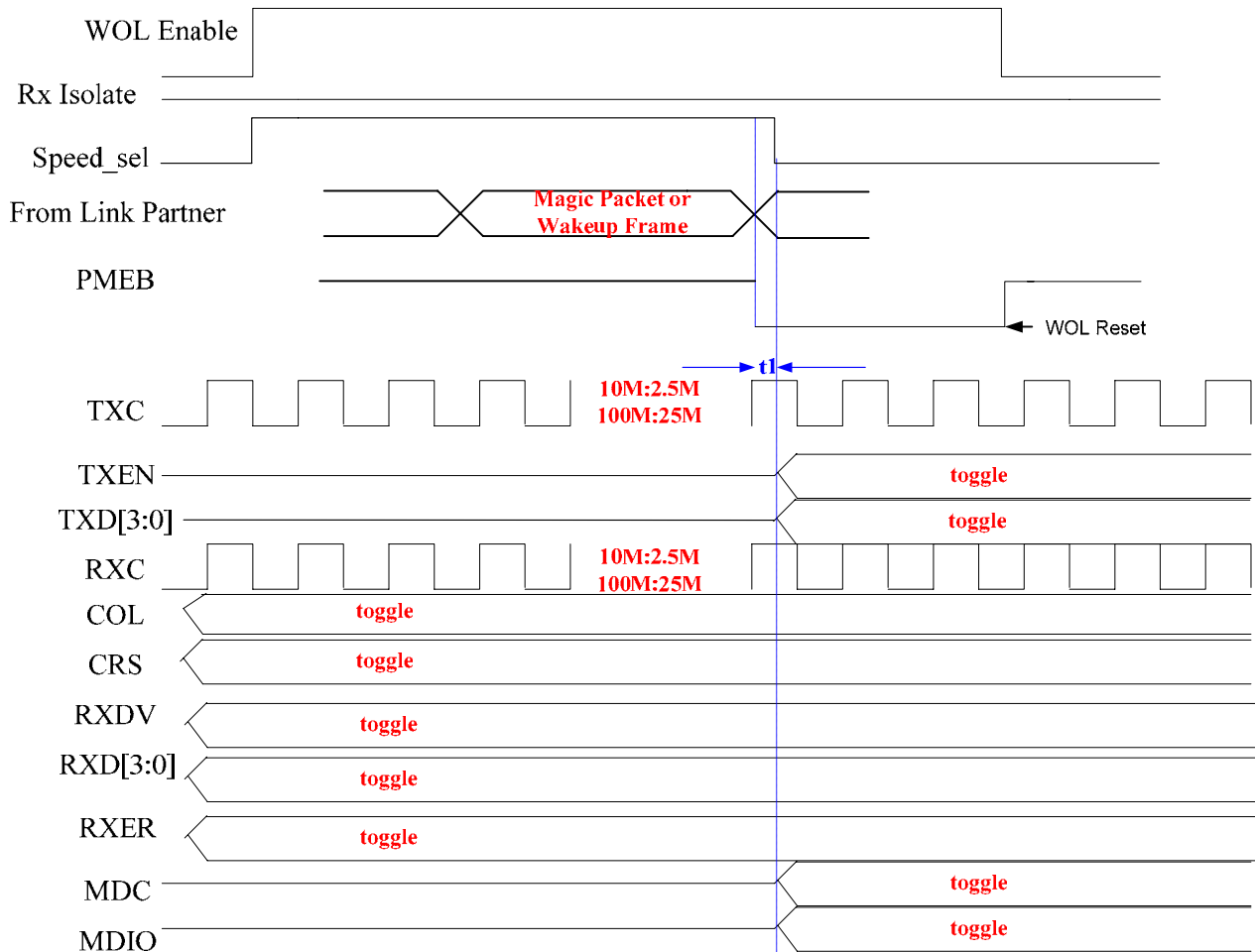**(Not Available for the RTL8201FR-VB)**



**Figure 15.   WOL Waveform with RX Isolate=0 and TX Isolate=0 in MII Mode (Active Low)**

*Note 1: Assumes that MAC TXEN, TXD [3:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: In MII mode we recommend setting TXC to toggle.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

*Note 5: PMEB Pin should be reset at WOL disable.*

*Note 6: PHYRSTB will be pulled high during WOL operation.*
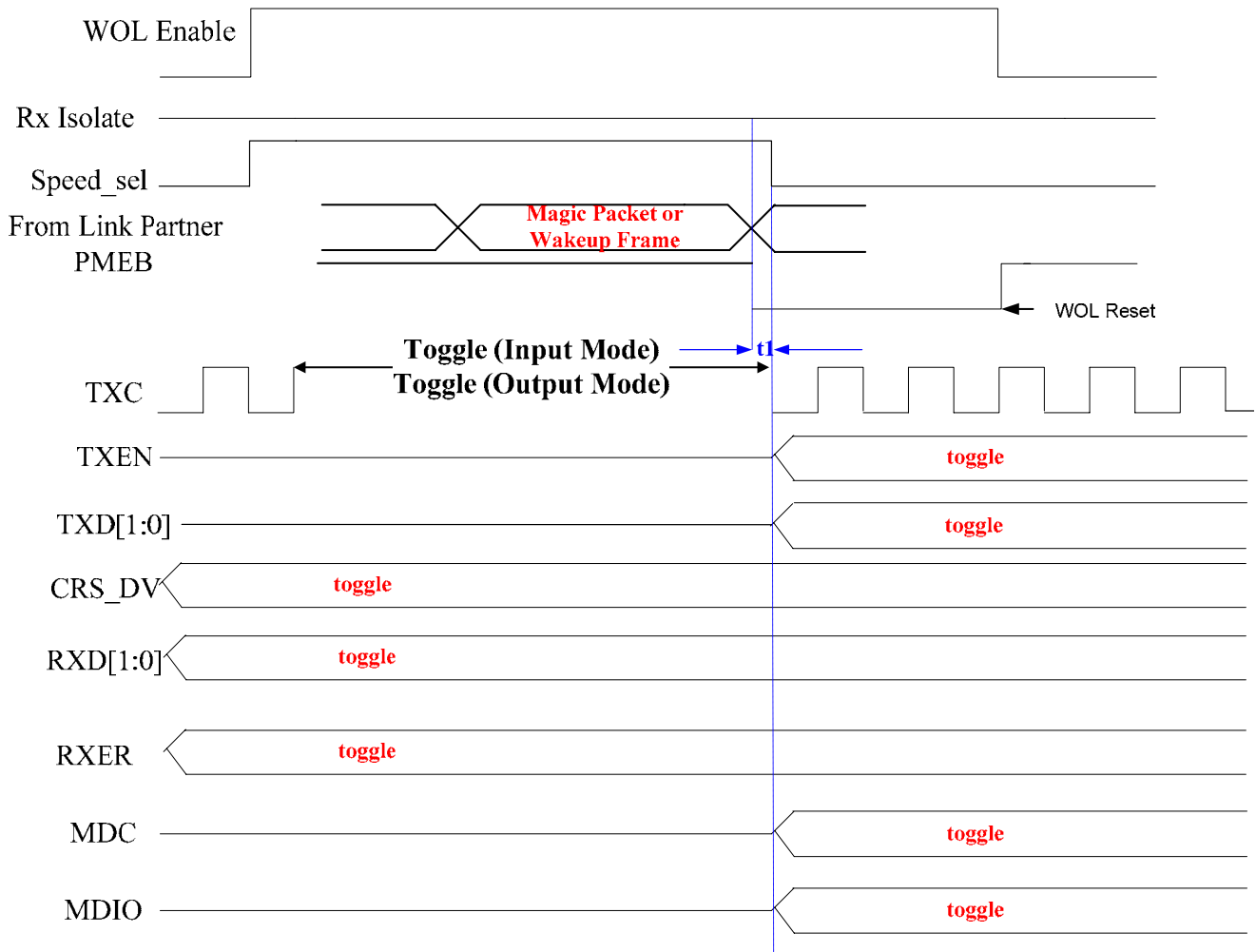
**RMII Mode -- PMEB Active Low After Receiving Magic Packet or Wake-Up Frame**



**Figure 16.   WOL Waveform with RX Isolate=0 and TX Isolate=0 in MII Mode (Active Low)**

*Note 1: Assumes that MAC TXEN, TXD [1:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: TXC cannot be halted in TXC input mode. TXC can be halted or kept toggling when TXC is in output mode.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

*Note 5: PMEB Pin should be reset at WOL disable.*

*Note 6: PHYRSTB will be pulled high during WOL operation.*

## 8.3. Pulse Low Wakeup

**Table 19.    Page 17, Reg19, Bit15 (RX Isolate Enable) (Pulse Low)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 19 | 15 | Rg_wol_rx_iso_en | RW | 0: Disable MII/RMII RX Isolate in WOL<br>1: Enable MII/RMII RX Isolate in WOL | 0 |

**Table 20.    Page 17, Reg19, Bit14 (RXC Halt/Toggle Selection) (Pulse Low)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 19 | 14 | Rg_wol_rxc_on | RW | Force MII Mode RXC ON when Enable MII RX Isolate<br>1: RXC toggle<br>0: RXC halt | 0 |

**Table 21.    Page 7, Reg20, Bit15 (TX Isolate Enable) (Pulse Low)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 20 | 15 | Rg_tx_iso_en | RW | Isolate MII/RMII TX when TX Idle<br>*Note: TX isolate can be used when the TX path is idle (not only for WOL).* | 0 |

**Table 22.    Page 17, Reg19, Bit [2:0] (PMEB Pulse Width & Active Low/Pulse Low Settings)**

| Reg | Bit | Name | Type | Description | Default Value |
|-----|-----|------|------|-------------|---------------|
| 19 | 2:1 | Rg_pmeb_pulse_width | RW | Pulse Width of PMEB Pin<br>00: 84ms<br>01: 168ms (Default)<br>10: 336ms<br>11: 772ms | 01 |
| 19 | 0 | Rg_pmeb_pulse_ena | RW | PMEB Active Low/Pulse Low Setting<br>1: Pulse Low wake-up<br>0: Active low wake-up | 0 |

## 8.3.1.    RX Isolate=1 (TX may or may not be set to isolated)

**MII Mode -- PMEB Pulse Low After Receiving Magic Packet or Wake-Up Frame**

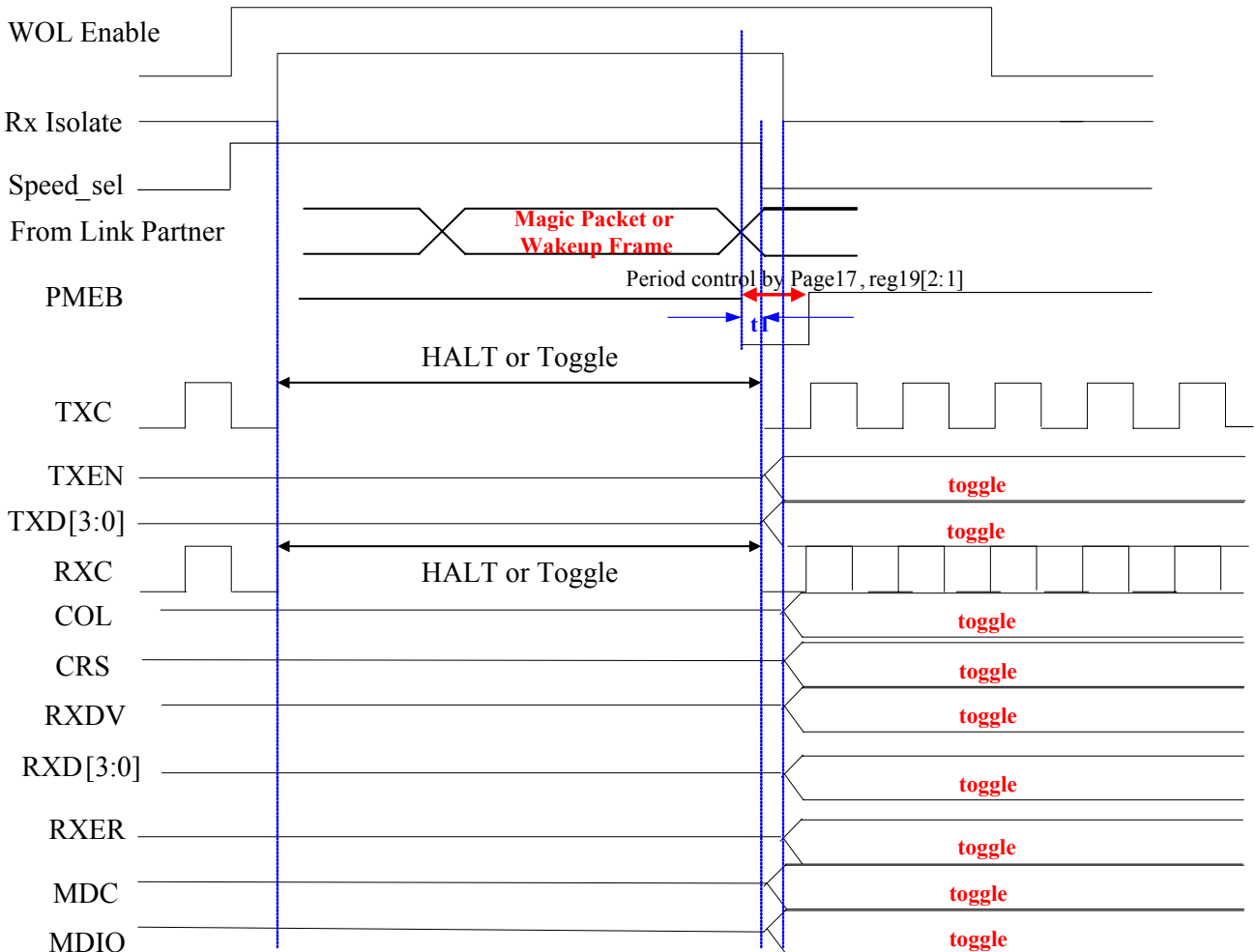**(Not Available for the RTL8201FR-VB)**



**Figure 17.    WOL Waveform with RX Isolate=1 in MII Mode (Pulse Low)**

*Note 1: Assumes that MAC TXEN, TXD [3:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: TXC and RXC can be halted or kept toggling in MII mode via register settings.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

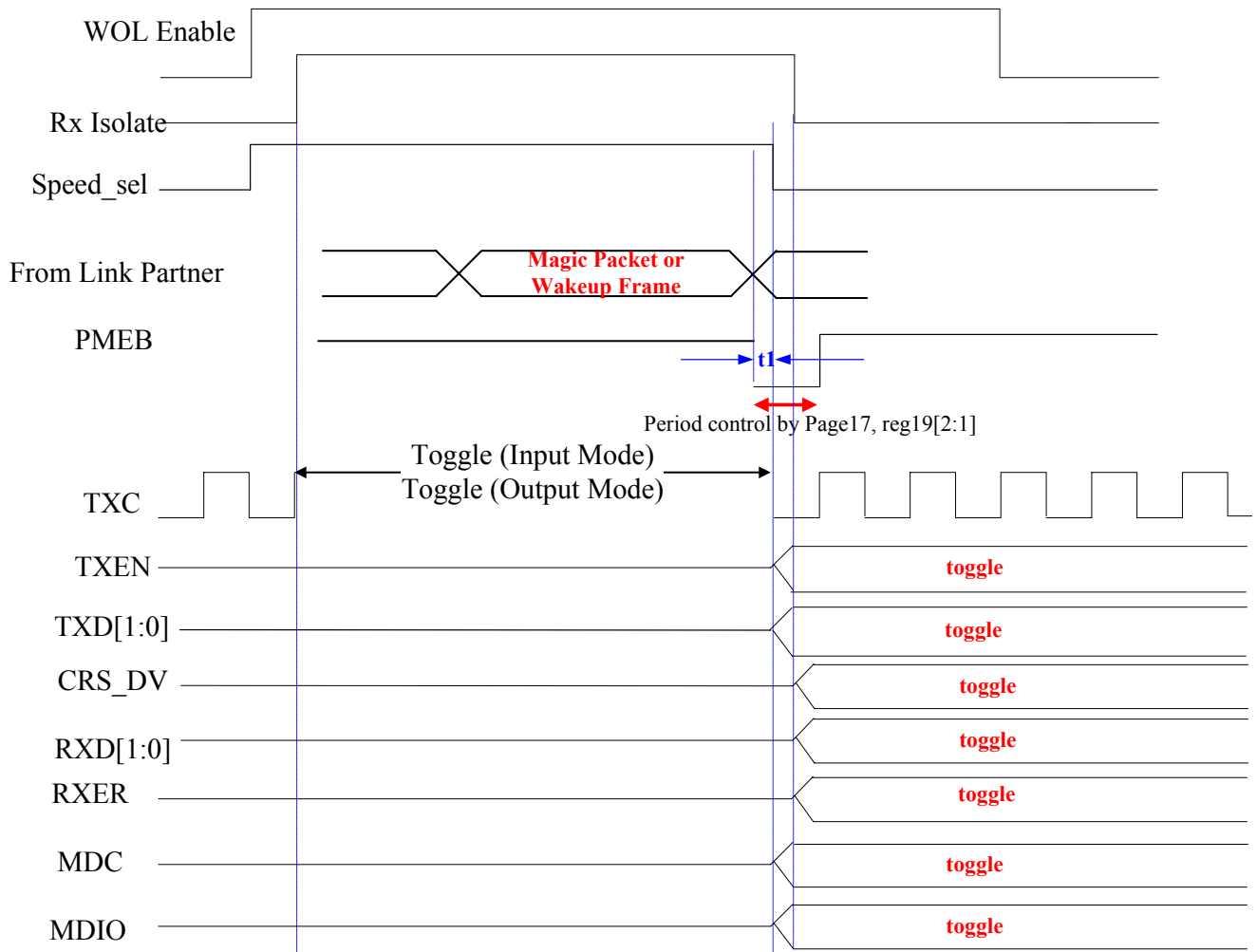*Note 5: PHYRSTB will be pulled high during WOL operation.*

**RMII Mode -- PMEB Pulse Low After Receiving Magic Packet or Wake-Up Frame**



**Figure 18.   WOL Waveform with RX Isolate=1 in RMII Mode (Pulse Low)**

*Note 1: Assumes that MAC TXEN, TXD [1:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: TXC cannot be halted in TXC input mode. TXC can be halted or kept toggling when TXC is in output mode.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

*Note 5: PHYRSTB will be pulled high during WOL operation.*

## 8.3.2.   RX Isolate=0 (TX Isolate=0)

**MII Mode -- PMEB Pulse Low After Receiving Magic Packet or Wake-Up Frame**

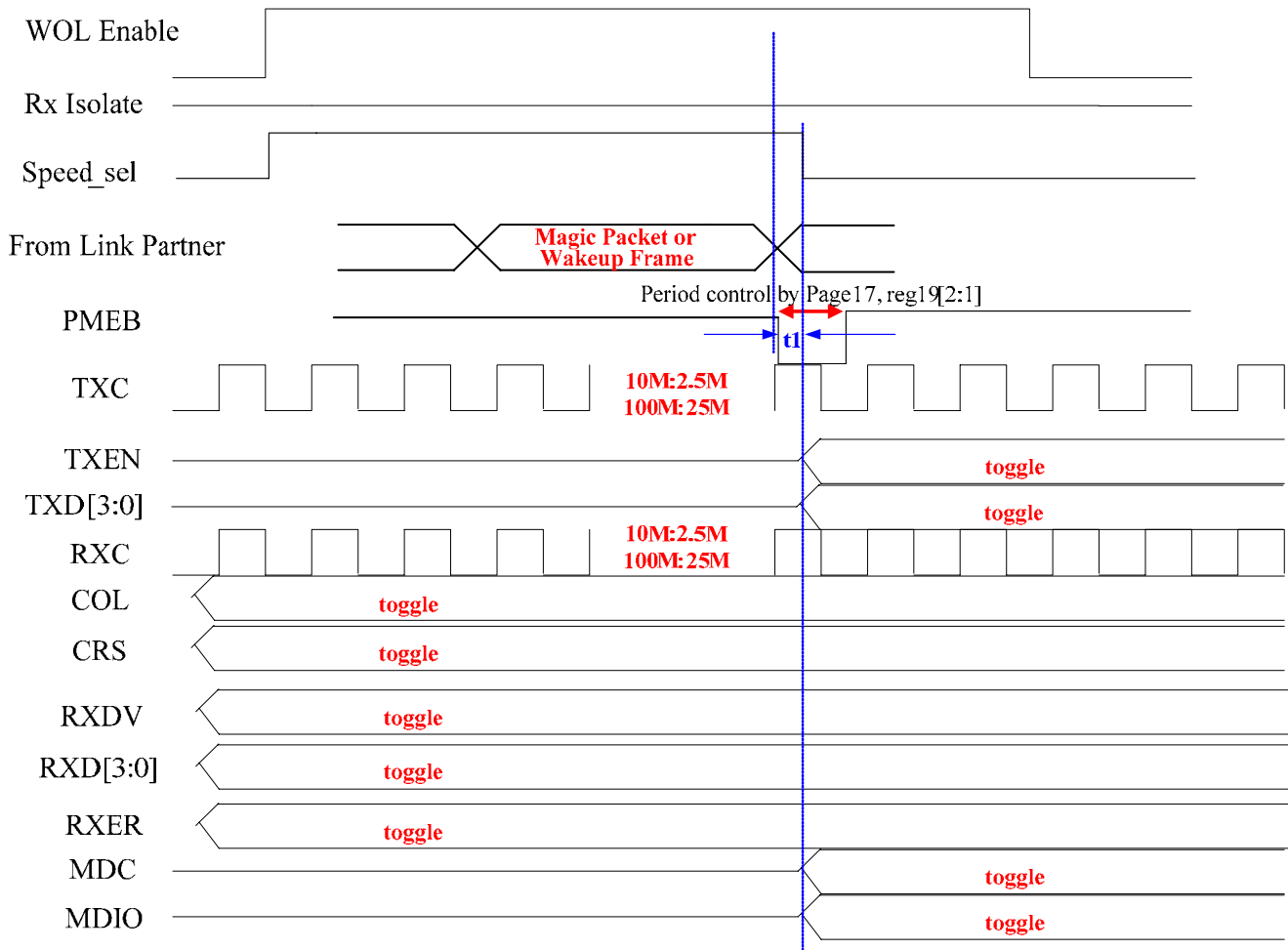**(Not Available for the RTL8201FR-VB)**



**Figure 19.   WOL Waveform with RX Isolate=0 and TX Isolate=0 in MII Mode (Pulse Low)**

*Note 1: Assumes that MAC TXEN, TXD [3:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: In MII mode we recommend setting TXC to toggle.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

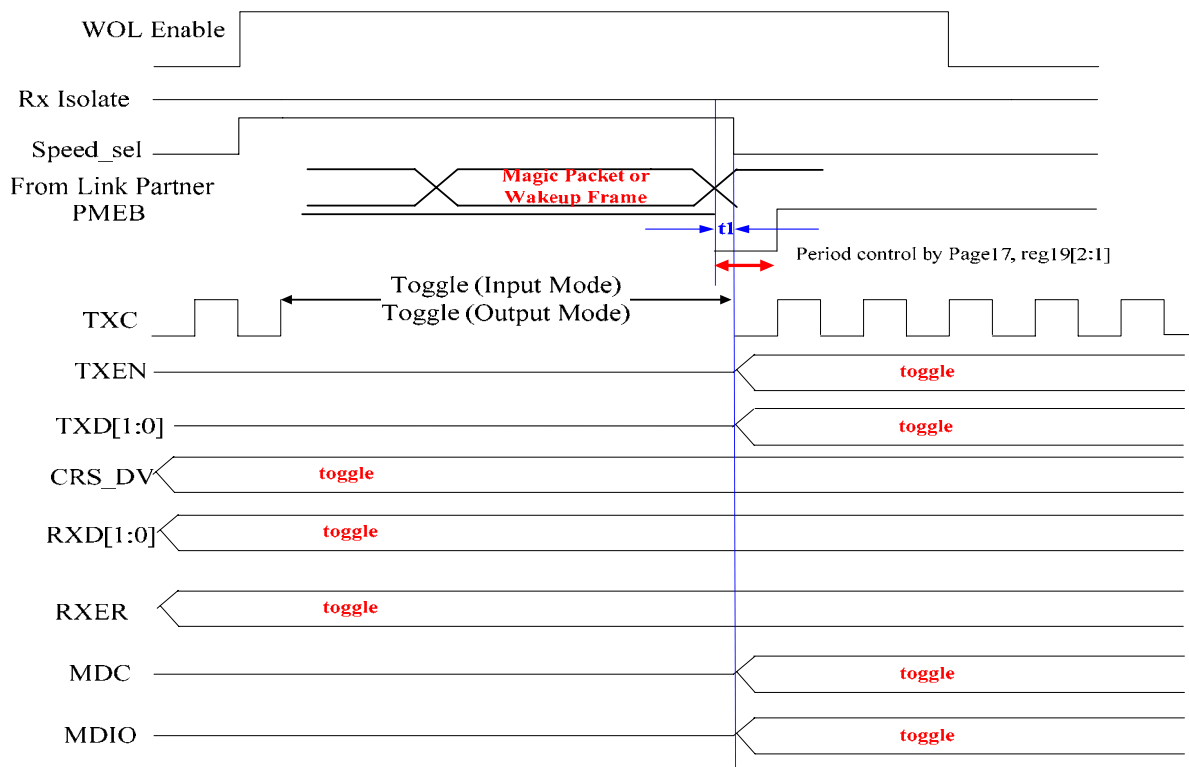*Note 5: PHYRSTB will be pulled high during WOL operation.*

## RMII Mode -- PMEB Pulse Low After Receiving Magic Packet or Wake-Up Frame



**Figure 20.   WOL Waveform with RX Isolate=0 and TX Isolate=0 in RMII Mode (Pulse Low)**

*Note 1: Assumes that MAC TXEN, TXD [1:0], MDC and MDIO are set to not toggle during MAC sleep.*

*Note 2: t1 is the MAC Wakeup time.*

*Note 3: TXC cannot be halted in TXC input mode. TXC can be halted or kept toggling when TXC is in output mode.*

*Note 4: Speed_sel=0 → MAC sets PHY speed=100M; Speed_sel=1 → MAC sets PHY speed=10M.*

*Note 5: PHYRSTB will be pulled high during WOL operation.*